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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/123,208 07/27/98 KIRIAKI

S TI-21556

MM32/1228

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EXAMINER

LE, T

ART UNIT	PAPER NUMBER
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2819

DATE MAILED:

12/28/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.
09/123,208

Applicant(s)
Kiriaki

Examiner
Thanh-Tam Le

Group Art Unit
2819



☒ Responsive to communication(s) filed on Jul 27, 1998

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire three month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-9 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1, 4, and 7 is/are rejected.

☒ Claim(s) 2, 3, 5, 6, 8, and 9 is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
☐ received.

☐ received in Application No. (Series Code/Serial Number) _____

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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DETAILED ACTION

Page 4, line 14 "o or" should be changed to --or--

Page 5, line 4, " be between" should be changed to --between--

Page 5, line 17, " the;" should be changed to --the--

Page 5, line 17, ";the" should be changed to --the--

Page 8, claim 3, line 7, "the said" should be changed to --said--

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Flannagan et al. (U.S. Patent 5,059,829).

Regarding independent claims 1, 4 and 7, in figure 3, Flannagan teaches all the features of the claimed invention including: apparatus and method for converting low level input signals to CMOS level output signals comprising: a pre-amplifier (202, 212 and 216) coupled to receive the low level input signals (V_{in} and V'_{in}) and for producing two output signals, the two output signals being at opposite logic levels; first and second output buffers each operatively coupled to receive a different of the two output signals, each of the first and second output buffers having an

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emitter follower transistors (210 and 214), with the load of the emitter follower provided by a second transistor (218 and 220); a circuit for providing different drive signals (228) for each of the second transistors (218/220), each the drive signal serving to turn off one of the second transistors (218/220) when the desired output of the corresponding emitter follower (210/214) is a preselected logic level.

Allowable Subject Matter

3. Claims 2, 3, 5, 6, 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is an examiner's statement of reasons for allowance:

The closest prior art of record, Flannagan et al. (U.S Patent 5,059,829) does not teach or suggest a apparatus and method for converting low level input signals to CMOS level signals comprising a pair of third transistors; a second buffer circuit or an intermediate buffer circuits.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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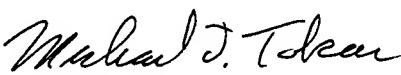
Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh-Tam (Tammy) Le whose telephone number is (703) 306-5711. The examiner's can normally be reached on Monday to Friday from 7:30AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Mike Tokar, can be reach at (703) 305-3493. The fax phone number for this group is (703) 305-3432.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

Tammy Le
Examiner, Art Unit 2819
12/07/1999


Michael Tokar
Supervisory Patent Examiner
Technology Center 2800